What is claimed is:

1. A MOS (Metal Oxide Semiconductor) transistor comprising:

a gate insulating film disposed on a surface of a silicon substrate comprising a central portion formed of a nitride insulating film containing at least nitrogen and both end portions located on both sides of said central portion, each formed of an oxide insulating film containing oxygen and no nitrogen;

a p-type gate electrode formed on said gate insulating film;

sidewalls formed on both sides of said gate insulating film and said gate electrode;

a pair of p-type source/drain areas formed in surface portions of said silicon substrate; and

a channel area located between said pair of source/drain areas.

2. The MOS transistor according to claim 1, wherein said source/drain area is of LDD (Lightly Doped Drain-Source) structure comprising lightly doped source/drain area located on inner side in contact with said channel area and deeply doped source/drain area located on the outer side of said lightly doped source/drain area.

3. The MOS transistor according to claim 1, wherein said oxide insulating film is thicker than said nitride insulating film.

4. The MOS transistor according to claim 2, wherein said oxide insulating film is thicker than said nitride insulating film.

5. The MOS transistor according to claim 3, wherein said nitride insulating film is formed of a silicon oxynitride film, and said oxide insulating film is formed of a silicon thermal oxidation film.

6. The MOS transistor according to claim 4, wherein said nitride insulating film is formed of a silicon oxynitride film, and said oxide insulating film is formed of a silicon thermal oxidation film.

7. The MOS transistor according to claim 1, wherein said oxide insulating film is formed integrally with said sidewall.

8. The MOS transistor according to claim 2, wherein said oxide insulating film is formed integrally with said sidewall.

9. The MOS transistor according to claim 1, wherein an interface between said gate insulating film and each of said sidewalls is close to an interface between said channel area and each of said source/drain areas.

10. The MOS transistor according to claim 9, wherein an interface between said nitride insulating film and each said oxide insulating film is close to an interface between said channel area and each said source/drain area.

11. The MOS transistor according to claim 2, wherein an interface between each of said lightly doped source/drain areas and each of said deeply doped source/drain areas is close to an outer side surface of each of said sidewalls.

12. A method of manufacturing a MOS transistor of LDD structure, comprising the steps of:

forming a nitride insulating film on a surface of silicon substrate;

forming a gate electrode in a predetermined pattern on a surface of said nitride insulating film;

performing wet etching of said nitride insulating film with said gate electrode used as a mask;

forming an oxide insulating film thicker than said nitride insulating film under each of both end portions of said gate electrode where said nitride insulating film is removed;

forming lightly doped source/drain areas in surface portions of said silicon substrate with said gate electrode used as a mask;

forming sidewalls on said lightly doped source/drain areas; and

forming deeply doped source/drain areas in surface portions of said silicon substrate with said sidewalls used as masks.

13. The method of manufacturing a MOS transistor of LDD structure according to claim 12, wherein said step of performing wet etching removes a portion of said nitride insulating film not masked by said gate electrode and removes portions of said nitride insulating film under both end portions of said gate electrode.

14. The method of manufacturing a MOS transistor of LDD structure according to claim 12, wherein said nitride insulating film is a silicon oxynitride film, and said oxide insulating film is a silicon thermal oxidation film formed through thermal oxidation.

15. The method of manufacturing a MOS transistor of LDD structure according to claim 13, wherein said nitride insulating film is a silicon oxynitride film, and said oxide insulating film is a silicon thermal oxidation film formed through thermal oxidation.

16. A method of manufacturing a MOS transistor of LDD structure, comprising the steps of:

forming a nitride insulating film on a surface of silicon substrate;

forming a gate electrode in a predetermined pattern on a surface of said nitride insulating film;

performing wet etching of said nitride insulating film with said gate electrode used as a mask;

forming lightly doped source/drain areas in surface portions of said silicon substrate with said gate electrode used as a mask;

forming sidewalls on said source/drain areas and an oxide insulating film integrally with said sidewalls under each of both end portions of said gate electrode where said nitride insulating film is removed by a CVD (Chemical Vapor Deposition) method; and

forming deeply doped source/drain areas in surface portions of said silicon substrate with said sidewalls used as masks.

17. The method of manufacturing a MOS transistor of LDD structure according to claim 16, wherein said step of performing wet etching removes a portion of said nitride insulating film not masked by said gate electrode and removes portions of said nitride insulating film under both end portions of said gate electrode.

18. The method of manufacturing a MOS transistor of LDD structure according to claim 16, wherein said nitride insulating film is a silicon oxynitride film, and said oxide insulating film is a silicon oxide film.

19. The method of manufacturing a MOS transistor of LDD structure according to claim 17, wherein said nitride insulating film is a silicon oxynitride film, and said oxide insulating film is a silicon oxide film.